WHAT IS CLAIMED IS

1. A method for compressing output data is characterized to write first data of a certain bit in a corresponding address of core cell regions, read the first data of a certain bit written in the address, compare the written data and the read data by dividing it to an upper certain bit and a lower certain bit, generate compressed data of 1 bit with an information about whether a fail is.

2. A method for compressing output data comprising :
a step for reading data from a core cell region and prefetching it to a first certain bit in a normal mode;
a step for writing first data of certain bit in a corresponding address of the core cell region in a test mode;
a step for reading the first data of certain bit written in the address of the core cell region and prefetching it;
a step for comparing the written data of certain bit and the read data of certain bit by dividing them to data of an upper certain bit and data of a lower certain bit;
a step for compressing a first error signal of certain bit to 1 bit data with an information about whether a fail is according to a comparing result and generating it;
a step for selecting first data of certain bit prefetched in a normal mode or the first error signal of certain bit in a test mode according to a control signal;
a step for shifting selected data of certain bit in an ascending edge and a descending edge of a clock signal and outputting them serially via a number of output pads in a normal mode;
a step for shifting selected data of certain bit in an ascending edge and a descending edge of the clock signal and outputting them serially via corresponding one of a number of output pads in a test mode.

3. The method for compressing output data as clamed in clame 2, wherein the first prefetched data of certain bit or the written and read data are 8 bits data, the 8 bits data are divided to upper 4 bits data or lower 4 bits data and compressed to 1 bit data with a fail information when it is a test mode.

4. A packet command driving type memory device comprising :
a read data comparing part for receiving and comparing first data of certain bit read from a core cell region and generating compressed 2 bits data;
a data input, output part for shifting the data compressed via the read data comparing part or the data read from the core cell region and transforming it to series data according to a clock signal;
an interface part for outputting the data read from the data input, output part according to the clock signal serially in a packet form via an output pad.

5. The packet command driving type memory device as claimed in claim 4, wherein the first prefetched data of certain bit are 8 bits prefetched data, the 8 bits data are divided into upper 4 bits data or lower 4 bits data, the upper or the lower 4 bits data are compressed to 1 bit signal.

6. The packet command driving type memory device as claimed in claim 4, wherein the read data comparing part comprises :
a number of comparators for receiving and comparing upper or lower 4 bits data of prefetched 8 bits data according to a control signal and generating 1 bit compressed data with a fail information respectively;
a selecting means for selecting the prefetched 8 bits data in a normal mode, and the compressed 8 bits data from a corresponding fourth comparator of the numbers of comparators

in a test mode according to the control signal.

7. The packet command driving type memory device as claimed in claim 6, wherein the respective comparator comprises :
a first to a fourth comparing means for receiving the written 4 bits data and the read 4 bits data and comparing them by 1 bit and generating a first to a fourth comparing signal according to the control signal;
a generating means for receiving the first to a fourth comparing signal generated from the first to a fourth comparing means and generating 1 bit compressed data with an information about whether a fail is.

8. The packet command driving type memory device as claimed in claim 7, wherein the first to the fourth comparing means comprises :
a first NAND GATE for receiving corresponding 1 bit signal of the written 4 bits data and the control signal respectively;
a second NAND GATE for receiving corresponding 1 bit signal of the read 4 bits data and the control signal;
a third NAND GATE for receiving outputs of the first and the second NAND GATE;
a first and a second NMOS Transistor having gates and drains receiving the outputs of the first and the second NAND GATE;
a first and a second PMOS Transistor connected in series between a power voltage and a source of the first and the second NMOS Transistor, having gates receiving the outputs of the first and the second NAND GATE;
a third PMOS Transistor having a gate receiving an output of the third NAND GATE and a source receiving a power voltage and drains connected between sources of the first and the second NMOS Transistor and drains of the first and the second PMOS Transistor;

generates the first to the fourth comparing signal respectively via sources of the first and the second NMOS Transistor connected commonly and drains of the first to the third PMOS Transistor.

9. The packet command driving type memory device as claimed in claim 7, wherein the generating means comprises a fourth NAND GATE for receiving the first to the fourth comparing signal generated from the first to the fourth comparing means and generating 1 bit compressed data with a fail information.

10. A packet command driving type memory device comprising :
a number of comparators for receiving and comparing 8 bits data read from the core cell region and generating 4 bits compressed data, receiving and comparing upper or lower 4 bits data of 8 bits prefetched data according to the control signal and generating 1 bit compressed data with a fail information respectively;
a selecting means for selecting the 8 bits prefetched data in a normal mode, and the compressed 8 bits data from a corresponding fourth comparator of the numbers of comparators in a test mode according to the control signal.

11. A packet command driving type memory device comprising :
a read data comparing part having a number of comparators for receiving and comparing upper or lower 4 bits data of 8 bits prefetched data according to the control signal and generating 2 bits comparing signal, a selecting means for selecting the 8 bits prefetched data in a normal mode, and the compressed 8 bits data from a corresponding fourth comparator of the numbers of comparators in a test mode according to the control signal;
a data input, output part for shifting the data compressed via

the read data comparing part or the data read from the core cell region and transforming it to series data according to a clock signal;

an interface part for outputting the data read from the data input, output part according to the clock signal serially via an output pad.